IN THE SPECIFICATION:

Please amend paragraph number **[0007]** as follows:

[0007] In a method for electrically testing a flip-chip semiconductor assembly in accordance with this invention, the assembly is tested using, for example, an in-line or ~~in-situ~~ in situ test socket or probes after one or more integrated circuit (IC) dice and a substrate, such as a printed circuit board (PCB), are brought together to form the assembly and before the IC dice are encapsulated or otherwise sealed for permanent operation. As a result, any problems with the IC dice or their interconnection to the substrate can be fixed before sealing of the dice complicates repairs. The method thus avoids the problems associated with conventional known-good-die (KGD) repairs. Also, speed grading can be performed while the dice are tested.

Please amend paragraph number **[0008]** as follows:

[0008] The assembly may be manufactured using a "wet" conductive epoxy, such as a heat-snap-curable, moisture-curable, or radiation-curable epoxy, in which case bond pads on the IC dice can be brought into contact with conductive bumps on the substrate formed of the epoxy for the testing, which can then be followed by curing of the epoxy to form permanent ~~die-to-substrate~~ die-to-substrate interconnects if the assembly passes the test. If the assembly does not pass the test, the lack of curing allows for easy repair. After ~~curing~~ curing, but before sealing of the IC dice, the assembly can be tested again to detect any interconnection problems between the IC dice and the substrate.

Please amend paragraph number **[0009]** as follows:

[0009] The assembly may also be manufactured using a "dry" conductive epoxy, such as a thermoplastic epoxy, for conductive ~~die attach,~~ die attachment, in which ~~case~~ case, the IC dice and the substrate can be brought together and the epoxy cured to form permanent die-to-substrate interconnections, after which the testing may take place. Since the testing occurs before sealing of the IC dice, repair is still relatively easy.

Please amend paragraph number **[0015]** as follows:

[0015] As shown in FIGS. 2 and 3, in a process 20 for manufacturing flip-chip semiconductor assemblies in accordance with this invention, a printed circuit board (PCB) 22 is indexed into a ~~die attach~~ die-attach station (not shown), where it is inserted into an in-line test socket 24 or contacted by probes 25. It will be understood by those having skill in the technical field of this invention that the invention is applicable not only to PCBs, but also to a wide variety of other substrates used in the manufacture of flip-chip semiconductor assemblies.

Please amend paragraph number **[0016]** as follows:

[0016] When conductive epoxy dots 26 or "pads" deposited on the PCB 22 at the die ends of die-to-board-edge conductive traces 30 are made from a "wet" epoxy (*i.e.*, a quick-cure epoxy such as a heat-snap-curable, radiation-curable, or moisture-curable epoxy), then integrated circuit (IC) dice 28 are pressed (active surfaces down) against the conductive epoxy dots 26 during flip-chip attach so electrical connections are formed between the dice 28 and the in-line test socket 24 or probes 25 through the conductive epoxy dots 26 and conductive traces 30 on the PCB 22. Of course, it will be understood that the invention is also applicable to other flip-chip die-attach methods including, for example, solder-based methods. It will also be understood that the dice 28 may be of any type, including, for example, Dynamic Random Access Memory (DRAM) dice, Static RAM (SRAM) dice, Synchronous DRAM (SDRAM) dice, microprocessor dice, Application-Specific Integrated Circuit (ASIC) dice, and Digital Signal Processor (DSP) dice.

Please amend paragraph number **[0019]** as follows:

[0019] During quick cure, the "wet" conductive epoxy dots 26 of the assembly 32 are cured, typically using heat, radiation, or moisture. The assembly 32 is then electrically tested again to ensure that the quick curing has not disrupted the interconnections between the dice 28 and the conductive traces 30 through the conductive epoxy dots 26 and the bumps (not shown) on the bottom surfaces of the dice 28. If quick curing has disrupted these interconnections, then

the assembly 32 proceeds to the rework station, where the connections between the bumps and the conductive epoxy dots 26 can be repaired. The repaired assembly 32 is then retested and, if it passes, it proceeds to encapsulation (or some other form of sealing) and, ultimately, is shipped to customers along with those assemblies 32 that passed this testing step the first time through. Of course, it should be understood that this invention may be implemented with only one test stage for "wet" epoxy assemblies, although two stages are preferable.

Please amend paragraph number **[0021]** as follows:

[0021] During testing, if the assembly 32 fails, then it proceeds to a rework station, where the bumps (not shown) on the bottom of the dice 28, the dice 28 themselves, or the interconnection between the bumps and the conductive epoxy dots 26 can be repaired. The repaired assembly 32 then proceeds to encapsulation (or some other form of sealing) and, eventually, is shipped to customers along with those assemblies 32 that passed the testing the first time through.

Please amend paragraph number **[0022]** as follows:

[0022] Thus, this invention provides a repair method for flip-chip semiconductor assemblies that is less expensive than the previously described known-good-die (KGD) based rework process, because it does not require the pretesting of dice that the KGD process requires. Also, the methods of this invention are applicable to testing for both internal die defects and ~~die-to-PCB~~ die-to-PCB interconnection defects, and to repairing interconnections between dice and a PCB in a flip-chip semiconductor assembly, whereas the conventional KGD process is not. In addition, these inventive methods do not waste burn-in resources, in contrast to the conventional KGD process previously described. Finally, this invention allows for early and convenient speed grading of flip-chip semiconductor assemblies.

Please amend paragraph number **[0023]** as follows:

[0023] As shown in FIGS. 4 and 5, in a process 40 for manufacturing flip-chip semiconductor assemblies in accordance with this invention, a printed circuit board (PCB) 42 is indexed into a ~~die attach~~ die-attach station (not shown), where it is inserted into an in situ test socket 44. It will be understood by those having skill in the technical field of this invention that the invention is applicable not only to PCBs but also to a wide variety of other substrates used in the manufacture of flip-chip semiconductor assemblies.

Please amend paragraph number **[0024]** as follows:

[0024] When conductive epoxy dots 46 or "pads" deposited on the PCB 42 at the die ends of die-to-board-edge conductive traces 50 are made from a "wet" epoxy (*i.e.*, a quick-cure epoxy such as a heat-snap-curable, radiation-curable, or moisture-curable epoxy), then integrated circuit (IC) dice 48 are pressed (active surfaces down) against the conductive epoxy dots 46 during flip-chip attach so electrical connections are formed between the dice 48 and the in situ test socket 44 through the conductive epoxy dots 46 and conductive traces 50 on the PCB 42. Of course, it will be understood that the invention is also applicable to other flip-chip die-attach methods including, for example, ~~solder based~~ solder-based methods. It will also be understood that the dice 48 may be of any type, including, for example, Dynamic Random Access Memory (DRAM) dice, Static RAM (SRAM) dice, Synchronous DRAM (SDRAM) dice, microprocessor dice, Application-Specific Integrated Circuit (ASIC) dice, and Digital Signal Processor (DSP) dice.

Please amend paragraph number **[0025]** as follows:

[0025] Once such electrical connections are formed, an electrical test is performed on the flip-chip semiconductor assembly 52 formed by the dice 48 and the PCB 42 using the in situ test socket 44. This test typically involves checking for open connections that should be closed, and vice versa, but it can also involve more, fewer, or different electrical tests as need dictates. If the assembly 52 fails the test, it is diverted to a rework station, where any dice 48 identified as

being internally defective or as having a defective interconnection with the PCB 42 can easily be removed and reworked, either by repairing the failing dice 48 themselves or by repairing conductive bumps (not shown) on the bottom surfaces of the dice 48 used to connect the dice 48 to the conductive epoxy dots 46 on the PCB 42. Once repaired, the assembly 52 returns for retesting and, if it passes, it is advanced in the process 40 for quick curing along with all assemblies 52 that passed the test the first time through.

Please amend paragraph number **[0026]** as follows:

[0026] During quick cure, the "wet" <u>conductive</u> epoxy dots 46 of the assembly 52 are cured, typically using heat, radiation, or moisture. The assembly 52 is then electrically tested again to ensure that the quick curing has not disrupted the interconnections between the dice 48 and the conductive traces 50 through the conductive epoxy dots 46 and the bumps (not shown) on the bottom surfaces of the dice 48. If quick curing has disrupted these interconnections, then the assembly 52 proceeds to another rework station, where the connections between the bumps and the <u>conductive epoxy</u> dots 46 can be repaired. The repaired assembly 52 is then retested and, if it passes, it proceeds to encapsulation (or some other form of sealing) and, ultimately, is shipped to customers along with those assemblies 52 that passed this testing step the first time through. Of course, it should be understood that this invention may be implemented with only one test stage for "wet" epoxy assemblies, although the two stages shown in FIG. 4 are preferable.

Please amend paragraph number **[0027]** as follows:

[0027] When the conductive epoxy dots 46 are made from a "dry" epoxy (*e.g.*, a thermoplastic epoxy), then the PCB 42 is indexed and inserted into the <u>in situ</u> test socket 44 as described above, but the dice 48 are attached to the PCB 42 using heat before the assembly 52 proceeds to testing. During testing, if the assembly 52 fails, then it proceeds to a rework station, where the bumps <u>(not shown)</u> on the bottom of the dice 48, the dice 48 themselves, or the interconnection between the bumps and the conductive epoxy dots 46 can be repaired. The

repaired assembly 52 then proceeds to encapsulation (or some other form of sealing) and, eventually, is shipped to customers along with those assemblies 52 that passed the testing the first time through.

Please amend paragraph number **[0028]** as follows:

[0028] Thus, this invention provides a repair method for flip-chip semiconductor assemblies that is less expensive than the previously described known-good-die (KGD) based rework process, because it does not require the pretesting of dice that the KGD process requires. Also, the methods of this invention are applicable to testing for both internal die defects and ~~die-to PCB~~ die-to-PCB interconnection defects, and to repairing interconnections between dice and a PCB in a flip-chip semiconductor assembly, whereas the conventional KGD process is not. In addition, these inventive methods do not waste burn-in resources, in contrast to the conventional KGD process previously described.